Radiation Imaging Detectors Using SOI Technology

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Radiation Imaging Detectors Using SOI Technology

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ABSTRACT

Silicon-on-Insulator (SOI) technology is widely used in high-performance and low-power semiconductor devices. The SOI wafers have two layers of active silicon (Si), and normally the bottom Si layer is a mere physical structure. The idea of making intelligent pixel detectors by using the bottom Si layer as sensors for X-ray, infrared light, high-energy particles, neutrons, etc. emerged from very early days of the SOI technology. However, there have been several difficult issues with fabricating such detectors and they have not become very popular until recently.

This book offers a comprehensive overview of the basic concepts and research issues of SOI radiation image detectors. It introduces basic issues to implement the SOI detector and presents how to solve these issues. It also reveals fundamental techniques, improvement of radiation tolerance, applications, and examples of the detectors.

Since the SOI detector has both a thick sensing region and CMOS transistors in a monolithic die, many ideas have emerged to utilize this technology. This book is a good introduction for people who want to develop or use SOI detectors.

KEYWORDS

radiation image sensor, silicon-on-insulator, SOI, X-ray diffraction, X-ray imaging, X-ray astronomy, high-energy particle physics, synchrotron radiation, pixel detector, CMOS, radiation tolerance, monolithic sensor, particle detector

Contents

Preface

Currently there are many kinds of smart silicon sensors around us such as optical cameras, temperature/pressure sensors, accelerometers, and so on. However, most X-ray sensors are still a composition of a bulky scintillator and optical device. Since the X-ray energy is detected through scintillation light (indirect detection), position and energy resolutions are limited. To get better performance, semiconductor sensors which directly detect electrons or holes generated by radiation have been developed. In most cases, both the sensors and readout electronics use silicon as a material, but they are produced in different substrates and bump bonded as a hybrid detector.

In modern high-energy physics experiments, silicon pixel detector is one of the most important detectors. It measures the track position of secondary particles which are created by the high-energy particle collisions, in micron order precision. Development of the pixel detector was started in the 1990's and widely used in the Large Hadron Collider (LHC) experiments at CERN. However, these detectors were also hybrids of Si sensor and LSI readout chip. Therefore, they are very expensive and hard to fabricate due to its millions of bumps.

Many people have tried to develop a monolithic radiation detector which has both sensors and electronics in a same die. Silicon-on-Insulator (SOI) technology was the first candidate to realize these demands. However, lack of technology and coupling effect between sensors and electronics make it difficult to realize.

The Japanese high-energy accelerator laboratory, KEK, was behind in the development of pixel detectors as were many semiconductor companies in Japan. Several Japanese companies has been involved in the development of SOI wafer and LSI process from the beginning. NTT LSI lab. developed the first commercial-level SOI wafers by using SIMOX process and OKI Electric Industry Co. Ltd. (later Lapis Semiconductor Co. Ltd.) was the first worldwide to mass produce SOI devices.

To catch up to the radiation pixel detector technology developed in Europe, we started an SOI pixel detector project in 2005 in cooperation with the Lapis. At that time, there were very few researchers with experience in silicon detector or design of LSI circuits, and people in the Lapis didn't have any experience in radiation detection. Furthermore, the market of radiation image detector is not so large, so there were several difficult times to continue the cooperation. However, enthusiasm of the involved people enabled us to complete the SOI radiation detector.

Since the initial cost of the semiconductor process is very expensive, we decided to open our process to all academic users worldwide. We have been operating Multi Project Wafer (MPW) runs, by collecting many designs, one or twice per year. In addition to Japanese researchers, several foreign researchers also joined the MPW runs. Coordination of the MPW run is not an easy task, but we believe it is important task to continue the SOI detector project.

Recognized for our activity, the Japanese government gave us some R&D funds for the 2013–2017 fiscal year. Our collaboration was expanded with this R&D budget, and now we can bring electronics and image sensor experts to our collaboration. Furthermore, the collaboration could involve researchers in other fields such as mass separator, medical, material science, and so on.

The First International Workshop on SOI Detector (SOIPIX2015) was held in June 2015, when about 100 people from all over the world gathered in Sendai, Japan. We hope this book will help to expand SOI pixel technology worldwide.

SOIPIX2015 workshop in Sendai, Japan (June 3-5, 2015).

Yasuo Arai and Ikuo Kurachi
January 2017

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We gratefully acknowledge people at Lapis Semiconductor Co., Ltd, especially Mr. Okihara, Mr. Kasai, Mr. Miura, and Mr. Kuriyama. Without their continuous efforts, the SOI detector would not have been built. We also thank all the members of SOI collaboration who were involved in many aspects of work, such as simulation, design, testing, and discussion.

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Yasuo Arai and Ikuo Kurachi
January 2017

CHAPTER 1

Introduction

Silicon pixel detectors are indispensable tools for modern reasearch in high-energy physics [1], medical equipments [2], space science [3], and many other fields. At present, the most popular radiation image sensor is built as a hybrid of sensor chip and readout IC chip with metal bump bonding [4, 5]. However, the hybrid sensor has many limitations in performance, such as position resolution, thick unwanted materials, low production yield, and high cost. Therefore, a monolithic active pixel detector that has both sensors and a readout circuit in a single silicon die and is fabricated through a conventional semiconductor process is demanded.

There are several kinds of monolithic sensors. Using a standard bulk Complementary Metal-Oxide-Semiconductor (CMOS) process is the most convenient and widely used method. However, it is difficult to make thick sensing regions in the standard CMOS process [6], and it does not necessarily have the desired properties such as radiation hardness. Silicon-On-Insulator (SOI) technology becomes popular for high-performance, RF, or low-power IC applications. In SOI wafer, the circuit layer is isolated from the substrate (handle wafer). The substrate is normally just a physical support of the wafer and just acts as a backplane of the top circuit. However, the handle wafer is also a good quality silicon wafer, so active elements or sensors can be created in the handle wafer. To get good sensitivity for X-ray or infrared light, a thick sensing region and low-leakage current is mandatory. This necessitates using a high-purity silicon wafer different from low-resistivity wafer used in the circuit layer. To detect α-ray, β-ray, or high-energy charged particles, back illumination and thin window are normally required. These requirements are also difficult to fulfill in standard bulk CMOS technology.

The idea of the SOI detector first appeared around the 1990s [7]. At first, the SOI wafer was fabricated with a separation by implantation of oxygen (SIMOX) technology [8] from low-resistivity p-type wafer. Therefore, the detector could not provide advantages of the fully depleted one. Several pioneering works were done [9–11] but it was difficult to make a good detector due to insufficient technology in the SOI wafer and process.

In 2001, the development of SOI detectors with high-resistivity handle wafer was started by a collaboration of Silicon Ultra Fast Camera for Gamma and Beta Sources in Medical Applications (SUCIMA) project [12–14]. It was the first successful work on SOI detectors with high-resistivity handle wafer. The handle wafers were manufactured by using bond-and-etch-back SOI (BESOI) technology. Unfortunately, the process technology used was rather obsolete (CMOS 3 μm technology), and it suffered from many technical problems.

A Japanese group led by KEK started SOI Pixel R&D in collaboration with Lapis Semiconductor Co., Ltd. (former company name was OKI Electric Industry Co. Ltd.) [15] in 2005. The company was the first supplier of the mass-produced SOI Large-Scale Integrated circuit (LSI) in the world [16, 17]. They have been using bonded wafers called UNIBOND^{TM} wafers made by Smart Cut^{TM} method [18–20], in which high-resistive and low-resistive wafers can be bonded, sandwiching a buried oxide (BOX) layer. The thin low-resistivity upper *Si* layer is used for circuit implementation, and the high-resistivity bottom wafer (handle wafer, substrate) is used as a sensor. At first the pixel process is developed using R&D line of 0.15 μm CMOS Fully-Depleted (FD)-SOI process [15], and then moved to 0.20 μm FD-SOI process of mass-production line [21, 22]. The group has been operating Multi Project Wafer (MPW) runs, open to academic users worldwide, approximately twice per year [23–25]. They have solved many issues for realizing SOI radiation detector in SOI technology and developed many kinds of detectors. Furthermore, to fulfill demanding requirements in actual experiments, many new techniques, such as nested well, double-SOI, stitching, and 3D vertical integration [26], are being developed. A review article exists about the past activities on SOI development [27].

Figure 1.1 shows the schematic view of the SOI pixel detector (SOIPIX). The SOI wafer is composed of a thick, high-resistivity substrate (sensor part) and a thin low-resistivity *Si* layer (CMOS circuitry) sandwiching a buried oxide (BOX) layer. After removing the top *Si* and the BOX layer in the region of the sensing node contacts, *p* or *n* dopant is implanted to the substrate. Then contact vias and metal connections from the *p*-*n* junction to the transistors are created. The main advantages of the SOI detectors are as follows.

- There is no mechanical bump bonding, so obstacles, which will cause multiple scattering, are eliminated and smaller pixel size is possible.
- Parasitic capacitances of sensing nodes are very small (~10 fF), so large conversion gain and low noise operation are possible.
- Full CMOS circuitry can be implemented in the pixel.
- The thickness of the sensing region can be adjusted for radiation species and application requirement.
- Since generated electron-hole drift with electric field, position resolution is very good as high as a few micron. This is far better than X-ray sensor using scintillator where scintillation light is emitted at 360°.
- The cross section of single event effects caused by radiation is very small. A latch-up mechanism, which destroys conventional bulk CMOS LSI, is absent.
- Unlike conventional CMOS process, there is no leakage path to bulk. Thus, SOI transistors are shown to work over a very large temperature range from below 1~600 K.

- The technology is based on industry standards, and one of most promising technology for future LSIs. Thus, further progress and lower cost are foreseeable.
- Emerging vertical (3D) integration techniques are a natural extension of the SOI technology, so a much higher integration density is possible.

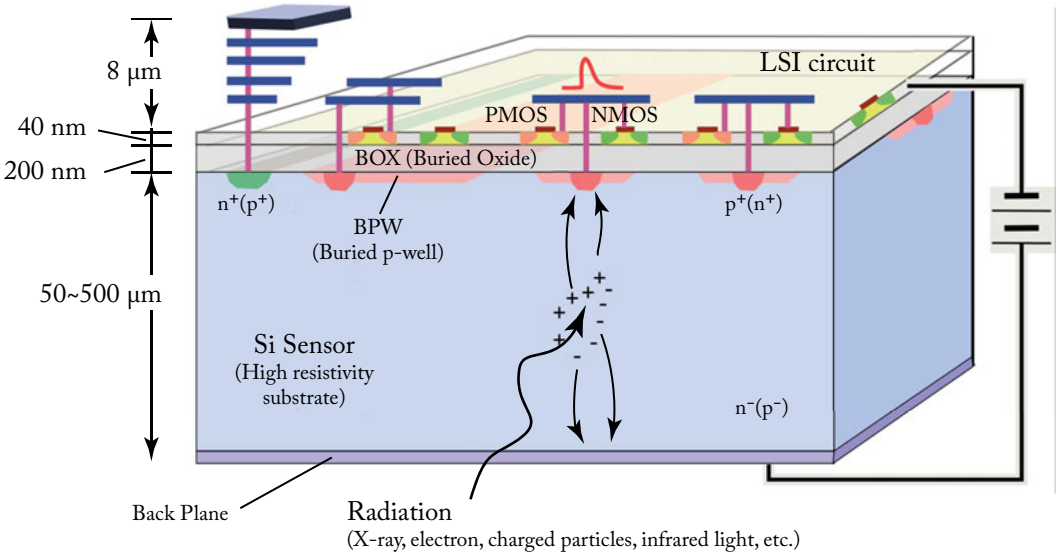

Figure 1.1: Schematic view of the typical SOIPIX.

The type of handle wafer can be either *n* or *p*, and doping impurity is changed according to the substrate type. We assume *n*-type substrate here otherwise noted.

To have good sensitivity, the depletion layer must have enough thickness and be depleted fully. Figure 1.2 shows X-ray detection efficiency for different silicon thickness. By using 500 μm thick silicon in full depletion condition, almost 100% detection efficiency is available for 10 keV X-ray, and 15% for 30 keV. When an X-ray interacts with silicon, a number of electron-hole pairs of (X-ray energy)/(3.65 eV) are created on average, so about 2700 e-h is available for 10 keV X-ray. For 1 keV X-ray, only 270 e-h is created and penetration depth is a few micro meters, therefore it is important to have a thin entrance window and low electronics noise. On the other hand, about 80 e-h/μm is created along with the track of high-energy charged particle. Thus, about 4000 e-h is available with only 50 μm thick sensor.

To deplete thick sensor with lower voltage, the dopant concentration in the handle wafer must be as low as 10^{12} cm^{-2}. For example, 200 V is necessary to fully deplete 10^{12} cm^{-3} (~4.5 kΩ•cm) *n*-type wafer of 500 μm thick. On the other hand, the dopant concentration in SOI circuit should be kept enough high as 10^{15} cm^{-3} to maintain the MOSFET characteris-

tics. Then, the SOI wafer made by wafer bonding method with Smart Cut^{TM} is preferable in the SOIPIX.

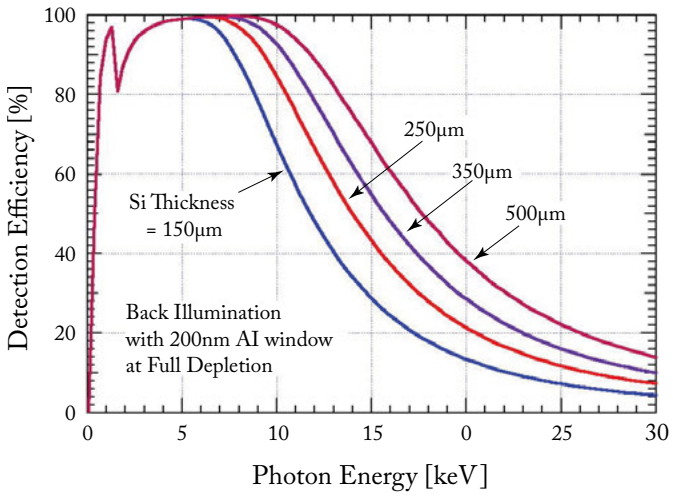

Figure 1.2: X-ray detection efficiency calculated from absorption length of *Si* sensor for different silicon thickness. The calculation assumes backside illumination through 200 nm Aluminum window and no dead layer in *Si*. For actual detection efficiency in a low-energy region, signal-to-noise ratio also limits the efficiency.

In Chapter 2, issues inherent in SOI pixel implementations are summarized, then in Chapter 3 technology to solve these issues mainly developed by KEK and LAPIS Co. Ltd. are introduced. In Chapter 4, we discuss radiation hardness of the SOI devices. In Chapter 5, recent R&D to expand the possibility of the SOIPIX such as stitching exposure and 3D integration are shown. In Chapter 6, various detectors developed so far are described.

CHAPTER 2

Major Issues in SOI Pixel Detector

In this chapter, major issues to realize SOI radiation detectors are presented. These are back-gate effect, crosstalk, leakage current, high-resistivity wafer process, and radiation hardness. Process modifications to solve these issues are described in Chapter 3 and radiation hardness issues are discussed in Chapter 4.

2.1 BACK-GATE EFFECT

The back-gate effect is one of the major difficulties with building a radiation sensor in SOI wafer [28–30]. Transistors are located very closely (~200 nm) to the sensor where high voltage is applied. The potential under the BOX acts as a back gate of the transistors. As the back-gate voltage is increased, the threshold voltage of the n-channel transistor (NMOS) is decreased and that of the p-channel transistor (PMOS) is increased, which will in the end cause the circuit not to work. Figure 2.1 shows an example of the threshold shifts in 0.15 μm SOI process.

2.2 CROSSTALK BETWEEN SENSORS AND CIRCUITS

For the SOI pixel detector, the BOX layer separates the electronics circuit and the sensor. Since the thickness of the BOX is very thin (~200 nm), voltage change in circuitry can induce signals in the sensors through capacitive couplings, and then signal oscillation may occur in some cases. Coupling path depends on the layout of pixel. Unfortunately, buried p-well (BPW) (Section 3.2.3) introduced to reduce the back-gate effect increases the capacitive coupling.

In integration-type pixels shown later, this coupling does not have any serious effect on the measurement. However, in counting-type pixel, this may have a large effect. In this case, differential signals and/or some sort of shielding between the sensors and circuits must be introduced. Thus, the nested well structure (Section 3.2.3) and double SOI technique (Section 5.1) are proposed and developed.

2.3 LEAKAGE CURRENT

During measurement, a leakage (dark) current flows into the sense node from the diode fabricated in the handle wafer. This increases the output voltage and noise. The leakage current of the sensor

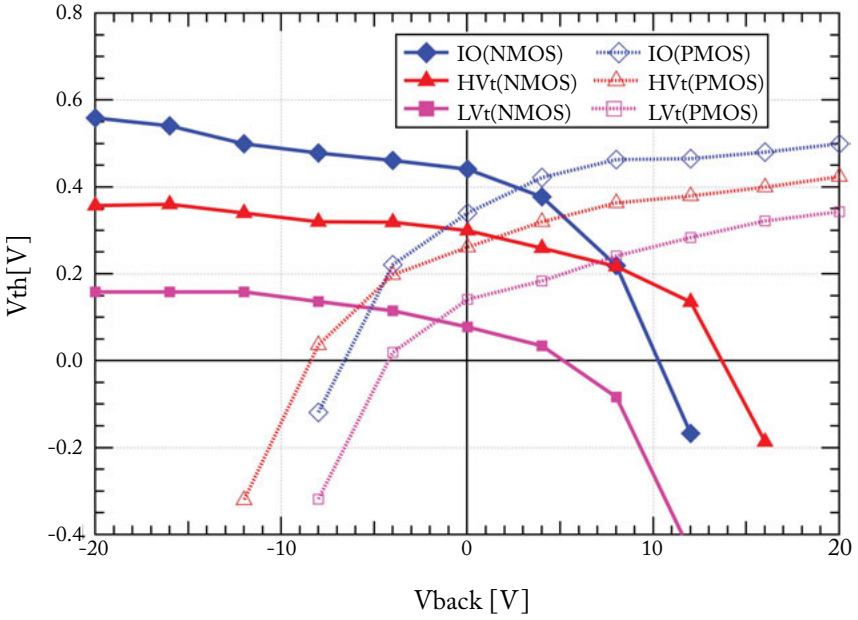

Figure 2.1: Measured threshold Voltage (Vth) shifts due to the back-gate voltage (Vback) for NMOS and PMOS transistors of the three different transistor type in 0.15 μm SOI technology.

is not so important for short integration time applications, but it is important for long integration time applications such as astronomical X-ray observation and measurements that require very good energy resolution.

The major leakage current comes from generation current in the depletion region, bonding interface between the BOX and substrate, and carrier diffusion from un-depleted region. These values strongly depend on manufacturer and wafer type. Low-temperature operation and buried p-n diode will help a lot to decrease the leakage current.

2.4 HIGH-RESISTIVITY WAFER

To have high-sensitivity for radiations and to get high-speed signal, a sensor must be depleted fully and excess voltage applied to speed up charge collection. The depletion depth is proportional to square root of ρ•V where ρ is resistivity of the wafer and V is applied voltage. Therefore, high-resistivity wafer is desirable to achieve full depletion with lower voltage. Usually Floating-Zone (FZ) wafer is used in a radiation sensor, but it is not easy to obtain large-size FZ wafers because of their processing difficulty and demand.

The handle wafer of the standard high-resistive SOI wafer is made in the Czochralski (CZ) method, which is n-type and has about 700 Ω•cm resistivity. KEK group made special SOI wafers